Nixon & Vanderhye P.C.
ATTORNEYS AT LAW

8TH FLOOR
1100 NORTH GLEBE ROAD
ARLINGTON, VIRGINIA 22201-4714

TELEPHONE: (703) 816-4000
FACSIMILE: (703) 816-4100
WRITER'S DIRECT DIAL NUMBER:
(703) 816-4029

FACSIMILE COVER SHEET
PLEASE DELIVER IMMEDIATELY!!!!

Our Ref.: 1035-243
Your Ref.: 09/487,259 Date: May 22, 2003

To: Examiner A. Mai
Firm: U.S. Patent and Trademark Office
Facsimile No.: 703-872-9318
From: Michael J. Shea

Number of Pages (including cover sheet): 16
(IF YOU DO NOT RECEIVE ALL OF THE PAGES OR ENCOUNTER DIFFICULTIES IN TRANSMISSION, PLEASE CONTACT US IMMEDIATELY AT (703-816-4000).

Debbie Phelps
FACSIMILE OPERATOR

ATTACHMENT/S: **Submission of Certified Translation and Request for Reconsideration**

MESSAGE:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

SASAKI

Serial No. 09/487,259

Filed: January 19, 2000

Title: METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE USING CHEMICAL ETCHING

Atty Dkt. 1035-243
C# M#

Group Art Unit: 2814

Examiner: A. Mai

Date: May 22, 2003

I hereby certify that this correspondence is being deposited with the United States Patent and Trademark Office, via facsimile, to Examiner A. Mai at (703) 872-9318, on May 22, 2003.

Signature

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

RESPONSE/AMENDMENT/LETTER

This is a response/amendment/letter in the above-identified application and includes an attachment which is hereby incorporated by reference and the signature below serves as the signature to the attachment in the absence of any other signature thereon.

☐ **Correspondence Address Indication Form Attached.**

Fees are attached as calculated below:

Total effective claims after amendment 42 minus highest number previously paid for 42 (at least 20) = 0 x $ 18.00		$	0.00
Independent claims after amendment 5 minus highest number previously paid for 5 (at least 3) = 0 x $ 84.00		$	0.00
If proper multiple dependent claims now added for first time, add $280.00 (ignore improper)		$	0.00
Petition is hereby made to extend the current due date so as to cover the filing date of this paper and attachment(s) ($110.00/1 month; $410.00/2 months; $930.00/3 months)		$	0.00
Terminal disclaimer enclosed, add $ 110.00		$	0.00
☐ First/second submission after Final Rejection pursuant to 37 CFR 1.129(a) ($750.00) ☐ Please enter the previously unentered , filed ☐ Submission attached		$	0.00
	Subtotal	$	**0.00**
If "small entity," then enter half (1/2) of subtotal and subtract ☐ Applicant claims "small entity" status. ☐ Statement filed herewith		-$	0.00
Rule 56 Information Disclosure Statement Filing Fee ($180.00)		$	0.00
Assignment Recording Fee ($40.00)		$	0.00
Other:			**0.00**
	TOTAL FEE ENCLOSED	$	**0.00**

The Commissioner is hereby authorized to charge any deficiency, or credit any overpayment, in the fee(s) filed, or asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Account No. 14-1140. A duplicate copy of this sheet is attached.

1100 North Glebe Road, 8th Floor
Arlington, Virginia 22201-4714
Telephone: (703) 816-4000
Facsimile: (703) 816-4100
MJS:dbp

NIXON & VANDERHYE P.C.
By Atty: Michael J. Shea, Reg. No. 34,725

Signature:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application:

SASAKI		Atty. Ref.:	1035-243
Serial No.:	09/487,259	Group:	2814
Filed:	January 19, 2000	Examiner:	A. Mai
For:	METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE USING CHEMICAL ETCHING		

* *

May 20, 2003

Assistant Commissioner for Patents
Washington, D.C. 20231

SUBMISSION OF CERTIFIED TRANSLATIONS AND REQUEST FOR RECONSIDERATION

Sir:

CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office (facsimile number 703-872-9318), on this the 22nd day of May in the year 2003.

Michael J. Shea

Michael J. Shea

Further to the Continued Prosecution Application filed April 30, 2003, reconsideration and allowance of the subject patent application are respectfully requested.

Applicant submits herewith a certification for the translations of JP 63-117445 and 7-161665.

Claims 1, 3-5, 9, 13 and 14 were rejected under 35 U.S.C. Section 103(a) as allegedly being unpatentable over Mutsumi *et al.* (JP 63-117445A).

As explained in the prior response, in Mutsumi *et al.* wax gets into the grooves between the chips thereby coating the cut faces with wax. In particular, Figure 2(d) of Mutsumi *et al.* illustrates that the wax gets into the grooves between the chips and Figure 2(f) shows adjacent chips adhered together by the wax n a post-etching step. When wax gets into the grooves between the chips, the sides of the chips damaged by dicing cannot be etched by etchant, even if the etching process removes the residual portions. In contrast, the method of claim 1 calls for, among other things, the chemical etching to remove damaged areas in a cut face of the semiconductor wafer resulting from the semi-full dicing process.

In response to these arguments, the office action alleges that page 4 of the Mutsumi *et al.* translation clearly discloses "[U]pon dicer test, cracks occur from these irregularities, and these cracks are developed by the machining distortions. Therefore, the chips after the dicing process is (sic) immersed in an etchant so that the machining-affected layer is removed so as to form a smooth surface." However, the aforementioned sentences are from the translation of Goto (JP 07-161665) rather than from the translation of Mutsumi *et al.* Thus, the "smooth surface of the machine-effected layer" to which the office action refers is that of Goto, not Mutsumi *et al.*

In summary, Applicant respectfully submits that the process set forth in Mutsumi *et al.* results in wax on the sides of chips subjected to semi-full dicing as explained at page 9-10 of the specification of the subject application:

> Moreover, in [Mutsumi *et al.*], chipping and cracks tend to occur due to breaking after washing, and since the cut face 107a, subjected to the semi-full dicing is coated with wax 117, it is not possible to carry out chemical etching on the cut face 107a after the dicing process, resulting in problems of fine cracks in the cut face, a machining-affected layer and chipping and cracking. In addition, in [Mutsumi *et al.*], a removing

> process for wax 117 is required, and the process after removal of the wax 117 has to be carried out on each piece of the semiconductor chips 107; therefore, a problem arises with working efficiency.

Thus, Mutsumi *et al.* does not teach or suggest that, *inter alia*, the damaged areas in a cut face of a semiconductor wafer resulting from a semi-full dicing process be removed by a chemical etching in which the residual portions are removed as claimed.

Accordingly, Applicant submits that claims 1, 3-5, 9, 13 and 14 are not obvious over Mutsumi *et al.*

Claim 2 was rejected under 35 U.S.C. Section 103(a) as allegedly being unpatentable over Mutsumi *et al.* in view of applicant admitted prior art (JP 07-022358) as to testing prior to semi-full dicing. However, testing prior to semi-full dicing does not remedy the above-identified deficiencies of Mutsumi *et al.* with respect to claim 1 (from which claim 2 depends). As such, Applicant submits that claim 2 is allowable.

Claims 10-13 and 15-19 rejected under 35 U.S.C. Section 103(a) as allegedly being unpatentable over Mutsumi *et al.* in view of applicant admitted prior art (JP 07-022358). JP 07-22358 discloses a process in which surface polishing is performed prior to a semi-full dicing process. JP 07-22358 also discloses that the rear face of a semiconductor wafer is affixed onto a dicing tape through a carrier frame. Among other things, JP 07-22358 does not remedy the above-identified deficiencies of JP 63-117445 with respect to claim 1 (from which claims 10-13 and 15-19 depend). As such, Applicant submits that claims 10-13 and 15-19 are allowable. In addition, JP 07-22358 fails to disclose features of at least some of claims 10-13 and 15-19. For example, claim 18 calls for the protective layer holding means to have a draining means for draining etchant. No such feature is shown in JP 07-22358 and the contention that such a feature is "inherent"

is conclusory. Claim 19 calls for the draining means to be formed as grooves extending in a radial direction. This feature is not shown and the argument in the office action that this feature does not appear to be critical does not establish its obviousness.

Claims 10-13 and 15-17 were rejected under 35 U.S.C. Section 103(a) as allegedly being unpatentable over Mutsumi *et al.* in view of Usami *et al.* (U.S. Patent No. 5,893,746). Usami *et al.* discloses a method of forming a semiconductor device in which a thin semiconductor wafer 105 is placed on a tape 107 held with a frame 101. This semiconductor wafer 105 is completely cut off by means of dicing grooves 104 and separated into a plurality of chips 105'. The separated chips 105' are pushed upwardly from the back side of tape 107 by means of a heating head 106 and is urged against a substrate 102 on which an adhesive 103 has been preliminarily applied, thereby causing the chip to be thermally bonded to the substrate 102. Among other things, Usami *et al.* does not remedy the above-identified deficiencies of Mutsumi *et al.* with respect to claim 1 (from which claims 10-13 and 15-17 depend). As such, Applicant submits that claims 10-13 and 15-17 are allowable.

The pending claims are believed to be in condition for allowance and early notification to that effect is respectfully requested.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 

Michael J. Shea
Registration No. 34,725

1100 North Glebe Road, 8th Floor
Arlington, Virginia 22201-4714
Telephone: (703) 816-4000
Facsimile: (703) 816-4100
MJS:dbp